



System-on-chip (SoC) devices which include microcontrollers (MCU), Application Specific Standard Products (ASSP) and Application Specific Integrated Circuits (ASIC), are evolving at a dramatic pace, with multiple cores, each running full operating systems, becoming more common. To get products based on such sophisticated devices to market on time requires an equally dramatic evolution in software development solutions

The ARM[®] RealView[®] tools being delivered today are a superior solution for current requirements and are already capable of meeting the evolving complex SoC design challenges. The flexible RealView tool solutions are designed to meet the requirements of SoC developers, designers of SoC-based products and developers of SoC product applications.

From the introduction of the original ARM core, ARM has been developing RealView tools in parallel with ARM processors and ARM on-chip debug solutions, ensuring a perfect complement between on- and off-chip system technology. These tools deliver the ultimate in software development solutions, ensuring the user can be confident of achieving significant time reductions in bringing products to market.

The RealView development solution provides all of the development tools required for present and future SoC device challenges.

The RealView development tools consist of:

- Software Development Tools
- Debug Hardware
- Hardware Platforms

RealView[®]
ARM[®] Tools by ARM

Software Development Tools

RealView Developer Suite

The ARM RealView Developer Suite provides a fully integrated software solution with leading edge tools for creating efficient software to run on any ARM processor. Servicing all major market segments, the RealView Developer Suite provides flexible software tools to meet present and future requirements.

The RealView Developer Suite includes:

- Fully optimizing ISO C/C++ compilers
- Powerful debug solutions
- High speed instruction set simulator

RealView Developer Suite — Compilation

The compilers within the RealView Developer Suite have been researched and developed for over 15 years to provide optimum support for the ARM architecture. The result is a robust and mature C/C++ compiler which continues to evolve with the expanding portfolio of ARM processor cores.

Reducing System Cost through Code Optimization

The RealView Developer Suite compilers use powerful optimizations to reduce the memory requirements of the application, allowing system designers to use smaller, less expensive memories. The following powerful optimizations are used to reduce the memory requirements of the application:

- Dead code elimination by the compiler
- Unused area elimination by the linker
- Support for packed data structures
- Peephole optimization using our knowledge of the ARM and Thumb® instruction sets
- Common sub-expression elimination

The RealView RVCT compilation tools provide advanced C++ features which have little or no memory requirements when not in use.

Reducing Power Consumption through Code Optimization

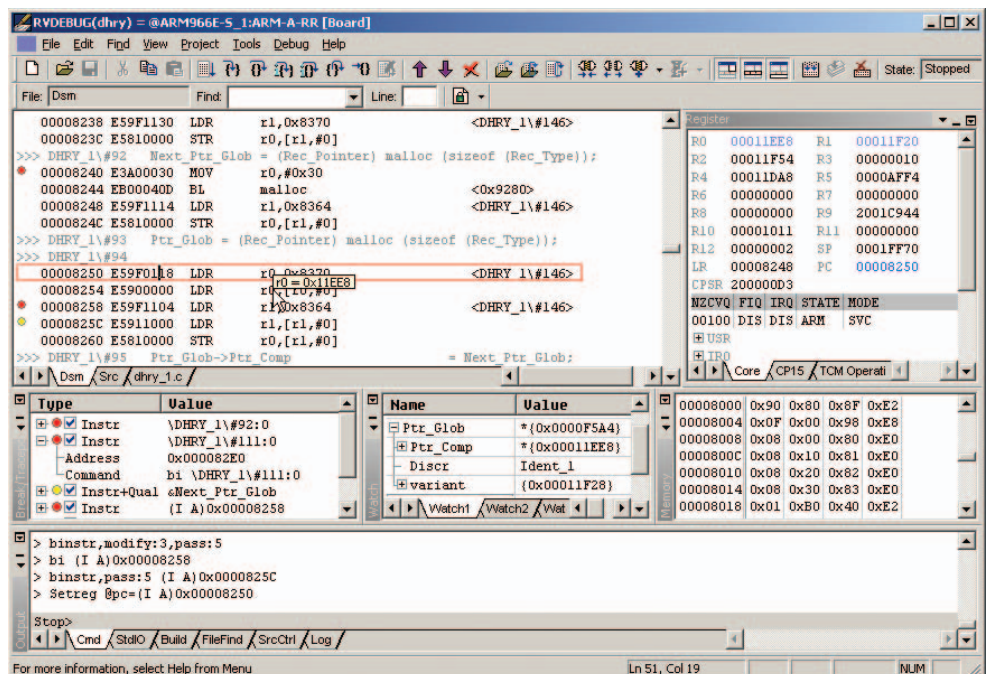
The RealView Developer Suite compilers deliver the maximum benefit from the renowned low power capabilities of ARM processors through a combination of performance and code size optimizations. The code size optimizations make better use of instruction caches and in general reduce code required to deliver desired functionality. Performance optimizations enable system functionality to be maintained at lower clock rates. Specific performance optimizations include:

- Loop body invariants
- Automatic inlining of suitable functions
- Tailcall optimization

- User can force inlining of chosen functions
- Placing small structs in registers
- Constant propagation
- Reducing constant divides
- Expression tree simplification
- Scheduling instructions to fit pipeline of specific ARM architecture/implementation

Selectable Compiler Revisions

RealView Developer Suite compilers are subject to continuous improvement in performance to support specific ARM cores. The RealView Developer Suite includes both current and previous versions of the compiler for organizations wishing to standardize their product families on a specific version.



Example screenshot of RVD debugger — source level debugging the ARM966E-S™

Hardware Platforms

RealView Integrator family

The RealView Integrator™ family is a range of baseboards and flexible development modules designed to meet the needs of SoC developers. The modular approach allows engineers to build custom development environments from known working sub-systems, therefore accelerating the design cycle.

Platform Baseboards

The Integrator/CP Compact Platform operates in conjunction with a Core Module to provide a fully integrated development platform. The Core Module FPGA implements a set of ARM PrimeCell® Peripherals and memory controllers. The PrimeCell Peripherals make use of the drivers and connectors on the baseboard. Expansion to Logic Modules and Logic Tiles is through an AMB™ AHB-Lite system bus.

For legacy designs, the Integrator/AP ASIC Development Platform supports all Core Modules and multiple Logic Modules or Logic Tiles. It is suitable for implementing multi-master designs around a single shared AMBA AHB system bus.

Core Modules

Core Modules can be operated standalone, in conjunction with Integrator Platform Baseboards, or in a stack with Logic Modules. Core Modules can also be used with third-party or user-designed platforms.

Logic Modules

Logic Modules provide uncommitted FPGAs connected to the AMBA system bus. They use the same form factor and connector layout as Core Modules and are designed to plug onto a platform baseboard or Core Module allowing users to prototype, test and integrate hardware IP.

Interface and Analyzer Modules

Interface Modules provide connectivity to real-world devices. The IM-AD1 is targeted at industrial and automotive applications. The IM-PD1 is targeted at consumer and portable devices. The IM-LT1 provides a transition between the RealView Integrator family and the new form factor and connector layout of the RealView Versatile family. The Analyzer Module allows the Integrator system bus to be observed using a logic analyzer.

RealView Versatile family

The RealView Versatile family is a new range of modular components comprising a platform baseboard and flexible development tiles. Characterised by high density, high speed and high levels of interconnect, the modular approach allows engineers to build custom development environments around the ARM PrimeXsys™ Platform architecture.

Platform Baseboard

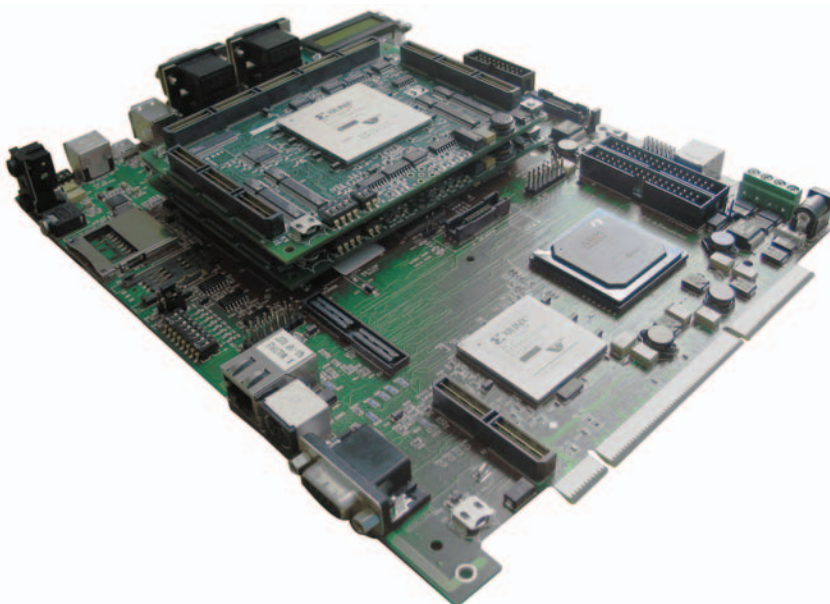
The Versatile Platform Baseboard for ARM926EJ-S™ is built around a highly integrated development chip, which includes memory controllers, peripherals required for OS booting, and 3D graphics acceleration hardware. The board provides all the standard interfaces required for software and hardware development, such as Ethernet, LCD display, USB and PCI. Expansion to Logic Tiles is through multi-layer AMBA AHB-buses.

Logic Tiles

Logic Tiles enable developers to prototype complete systems, prove custom IP, develop and test device drivers. Logic Tiles may be stacked to provide additional capacity. High performance and high pin-count interconnect allows large design prototyping. Although they are a Versatile family product, Logic Tiles can be used with Integrator family through the IM-LT1 Interface Module.

Interface and Analyzer Tiles

Interface Tiles provide connectivity to real-world devices. The first, called the Versatile/IT1, includes a prototyping area and a number of line drivers for typical applications such as USB and CAN bus, along with analogue inputs and outputs. The Analyzer Tile allows all signals between Logic Tiles to be observed using a logic analyzer.



RealView Developer Suite — Debug

The debuggers shipped within the RealView Developer Suite provide C/C++ and Assembler source level debugging via an easy-to-use, context sensitive, mouse driven GUI. The RealView AXD debugger ensures established development tool flows can be maintained whilst RealView RVD debugger provides advanced features such as multi-core debug, OS awareness and extended target visibility. The debuggers connect to run control units, with trace capture options or to the RealView RVISS instruction set simulator for code development prior to silicon availability.

The RealView debug tools reduce development time by allowing developers to debug at the level at which they generated their code — at assembler, high-level-language or OS process and thread level.

The debug tools provide flexibility, allowing freedom of choice from different silicon vendors, OS and Application Libraries vendors. The capability of the debug tools allows both low volume ASSP-based products and high-volume ASIC-based products to re-use a common tool chain, comprising:

- Simple and complex breakpointing
- Sophisticated watchpointing
- Stack rewinding
- Multiple synchronized debug perspectives
- Advanced data display, formatting and editing

RealView Developer Suite — Instruction Set Simulator

Providing a fully integrated, ARM core model-based, virtual development platform, the RVISS instruction set simulator offers models of ARM cores and ARM peripherals, and enables the development and simulation of user peripherals and memory systems.

The RVISS instruction set simulator within the RealView Developer Suite helps shorten the design cycle by enabling early device driver and application software development on a high performance virtual development platform for ARM core-based systems.

RealView Developer Suite

Optimizing ISO C Compiler Optimizing ISO C++ Compiler Assembler

- Compilation for both 16-bit Thumb and 32-bit ARM instruction sets
- Selectable debug and optimization levels
- Object files conform the ABI (Application Binary Interface) the ARM architecture, based on industry standard ELF and DWARF
- Powerful macro assembler for ARM and Thumb instruction sets

Linker

- Seamless inter-working of ARM and Thumb object code
- Scatter-loading feature supports placement of code and data within complex target memory maps
- Removal of unreferenced code areas and functions

ARM Object file Librarian/Archiver

- Enables sets of ELF object files to be collected together and maintained in libraries.
- Supports merging of libraries

Image Conversion Tool

- Converts from ELF images into binary, Motorola 32-bit S-record, Intel Hex-32 and Byte Oriented Hex formats
- Displays information about the input file, e.g., disassembly output or symbol listings

C and RogueWave C++ Libraries

- Functions defined by the ISO C library standard
- Target-dependent C library functions can be re-implemented for any execution environment
- The RogueWave C++ Standard Template Libraries

Debugger

- Source level debug through multi-windowed GUI
- Consumes ELF/DWARF images from the RealView compilers, images from supported DSP compilers, and other ARM ELF/DWARF compliant compilation tools that comply to the ABI for the ARM architecture
- SoC device JTAG connection through RealView ICE and Multi-ICE®
- Optional trace and analysis support for SoC devices with ETM™ (Embedded Trace Macrocell™) through RealView Trace and MultiTrace™
- OS aware debugging
 - Increasing number of OS/Application Libraries
 - Halted and Running System debug capability
- Advanced options for debug of multiple ARM cores and ARM + DSP (DSP vendor support may be required)
 - Multiple processor windows within the same debugger kernel
 - High integrity synchronized debugging
- Connects to RVISS instruction set simulator for early code development prior to silicon availability

Instruction Set Simulator

- Models of all current ARM cores
- Users can add their own memory and peripheral models
- Cycle-count information
- Easily customizable memory configuration to match target system

An evaluation version of the RealView Developer Suite is available on CD.

To request, please visit the ARM website at:

<http://www.arm.com/products/DevTools/RVDSEvalCD.html>

Debug Hardware

RealView ICE

Delivering industry leading performance, RealView ICE is the foundation of a modular solution that provides a network connected (10/100 Ethernet) run control unit that supports high speed program download and stepping for optimal productivity. RealView ICE delivers high-performance emulation through a standard JTAG port and supports a wide range of clock frequencies.

- Supports ARM Powered® devices with EmbeddedICE® macrocell and industry-standard JTAG connection
- Support for variable JTAG clock frequencies, 12.5Hz to 20 MHz (standard cable) or 50 MHz (LVDS cable)
- High-speed download: up to 500 KBytes/sec @ 10MHz JTAG clock
- Wide range of target voltages supported — 1.0 V to 5.0 V
- User I/O pins
- Support for all ARM cores, including ARM7™, ARM9™, ARM9E™, ARM10™ and ARM11™
- Control unit for RealView Trace

RealView Trace

RealView Trace is an expansion module for RealView ICE and shares its network connection to the host computer. RealView Trace interfaces with ARM ETM's for the ARM7, ARM9, ARM10 and ARM11 and in conjunction with the RVD debugger provides non-intrusive real-time tracing of instructions and data at over 250 MHz.

- Up to 8 million frames (no timestamp)
- Up to 4 million frames (with timestamp)
- 48-bit time stamp, 10 ns resolution, 32 day duration
- Fast on-the-fly trace data upload
- Fully variable trigger position
- ETM trace port modes supported
 - ETM protocols v1.x, v2.x, v3.x for ETM7™, ETM9™, ETM10™ and ETM11™
- Single and double edged clocking
- Normal, multiplexed and demultiplexed ports
- 4,8,16-bit data port widths

Multi-ICE

Multi-ICE is the industry standard solution for debug connections to ARM processors. It can be used in conjunction with all ARM debuggers included in the RealView Developer Suite, and a wide range of third-party debuggers. Multi-ICE utilizes a parallel port connection to a host PC, and enables debugging either locally or from another networked debug host.

- Supports ARM Powered devices with EmbeddedICE Macrocell and industry-standard JTAG connection, ARM7, ARM9 families, ARM1020E, ARM1022E
- Support for variable JTAG clock frequencies, 20 KHz to 10 MHz
- Download: 130 KBytes/sec @ 10 MHz JTAG clock
- Wide range of target voltages supported — 1.0 V to 5.0 V

MultiTrace

MultiTrace captures information from the trace port of SoC devices containing an ETM. MultiTrace buffers then sends the information via an Ethernet 10/100baseT connection to the host debug tools (RVD debugger or AXD debugger).

- Collects trace information at clock speeds up to 200MHz
- Works in conjunction with Multi-ICE to provide real-time trace functionality
- Supports data port widths of 4-, 8- and 16-bit, with records depths of 1M, 512K and 512K respectively
- Time stamps trace information: 48-bit with 10 ns resolution
- Compatible with the ETMs for ARM7, ARM9 core families, and ARM1020E™, ARM1022E™ cores



Supported Cores

The RealView development tools support the following ARM core families, and will also support ARM processor cores that are currently in development

- ARM7
- ARM9
- ARM9E
- ARM10
- ARM11
- Intel® XScale™ and StrongARM®

RealView debug development tools support the following non-ARM core-based families:

- Ceva OakDSP
- Ceva TeakLite
- Motorola M56621

Host Support

- Windows
- Linux
- Solaris

RealView Developer Suite Add-on Options

Multi-Core Mixed Architecture Debug

The RVD debugger provides the facility to debug multiple ARM cores or multiple ARM plus DSP cores using a single debug environment. Multiple windows are available for numerous processors and views. Each processor can be independently single stepped and breakpointed. Using a common debug kernel, facilities such as multi-core synchronized starting, stopping and stepping (in lock step) are available for examining and debugging the interaction between the applications running on the different cores on the system.

Cross triggering of multiple cores is supported in software and in hardware (where implemented). This facilitates the synchronous stopping of multiple cores when a breakpoint is hit on any of the

processors. These features allow the entire system to be paused to examine the state of each core, preventing data from being processed (lost) while examining the state of the multi-core system.

Ceva OakDSP/TeakLite Debug

The Ceva OakDSP/TeakLite debug add-on enables heterogeneous, multi-core debugging of ARM + OakDSP and ARM + TeakLite systems with any number of ARM, OakDSP, and TeakLite cores. This add-on supports all revisions of the OakDSP and all revisions up to revision B of TeakLite.

Motorola M56621 DSP Debug

The Motorola M56621 DSP debug add-on enables heterogeneous, multi-core debugging of ARM + M56621 DSP for the Motorola Neptune systems.

Documentation

The RealView Developer Suite, contains online documentation for all tools produced in DynaText 4.1 (except Linux) HTML documentation for the RogueWave C++ library is also available on the CD. Printed documentation is available for purchase separately.

Debug and Hardware Platforms have documentation included as standard.

Support

ARM understands how important technical support can be. As a result, all new products purchased from ARM come with an initial 12 months support and maintenance agreement (unless specified). To receive the continued backing of our support group during on-going development, 12 month support extensions at 20% of the product's list price can be purchased. For further information please contact support-renewals@arm.com.

Standards

Application Binary Interface for the ARM architecture

The Application Binary Interface (ABI) for the ARM Architecture enables interoperability of ARM executables within different toolchains, without recompilation. Users of ARM ABI compliant toolchains are able to use any debugger with any compiler, allowing binary code — such as libraries, to be re-used without re-compilation. More information about ARM's ABI support can be found at: <http://www.arm.com/products/DevTools/ABI.html>.

Further Information

Further information can be found at www.arm.com or by emailing realview@arm.com. ARM RealView products can be purchased from a worldwide distribution network or directly from ARM.



RealView®
ARM® Tools by ARM